

Performance Limits in Visible and Infrared Imager Sensors

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Abstract

Emerging CMOS image sensors are fundamentally superior to CCD imagers with respect to read noise and sensitivity at video data rates. We discuss each technology's performance limits, show that CMOS's advantages increase with the number of pixels, report supporting data and conclude that CMOS will likely supplant CCDs for megapixel imagers. CCDs can perform at their theoretical limit with minimum read noise of $\sim 1 e^-$ at 20 kHz data rate and 10-20 e^- at ~ 10 MHz. CMOS-based image sensors, on the other hand, can provide higher sensitivity and lower read noise at ≥ 10 MHz via pixel-based amplification bandwidth.

I. INTRODUCTION

Ubiquitous in consumer cameras through scientific instruments, the charge-coupled device (CCD) remains the prevalent imager technology for visible cameras. CCD technology has persevered over the last two decades because it detects, stores, delays and reads out analog signals with relatively low noise [1] and high uniformity. While astronomers have successfully lowered CCD read noise to 1 e^- [2] by constraining the video bandwidth to tens of kHz, the concomitant slow frame rates are acceptable mainly for imaging celestial scenes in the interest of science.

Though the CCD is still a workhorse for visible imaging and capture, the MOS-based technology it supplanted is now making a dramatic comeback due to the availability of submicron mixed-signal CMOS. Presaging this technology shift in visible sensors, infrared focal plane array (FPA) designers migrated to CMOS in the late 1980's. The available $\sim 2\mu\text{m}$ processes available at that time enabled robust pixel-based amplification in the relatively large infrared pixels (18 to $100\mu\text{m}$) and flip-chip hybrid architecture. The relative ease at which near-Nyquist bandlimiting is achieved with pixel-based amplification has enabled IR imagers with read noise below ten electrons [3]. By virtue of deep submicron CMOS, each visible CMOS imager pixel contains a photodetector with large optically active area ($>40\%$) and a low-noise amplifier in $<4\mu\text{m}$ pitch [4]. CMOS also facilitates system-on-a-chip integration, low power dissipation, and a competitive wafer fabrication infrastructure.

Figure 1 [5] illustrates the chronology of visible and infrared imager development over the last three decades versus an approximate timeline for MOS/CMOS process availability. Shown are the corresponding times when MOS, CCD, infrared focal plane array and CMOS visible imagers

of various pixel counts were successively introduced. Since $0.5\mu\text{m}$ is mature and $0.25\mu\text{m}$ now readily available, the progression in visible CMOS imager array size is driven by application need rather than lithography availability. The development rate is similar to that experienced when CCDs rapidly progressed to TV-compatible format at Bell Labs, RCA and Fairchild.

We show that the emerging CMOS imagers can have lower temporal noise than competing CCDs at video rates. This advantage increases with the number of pixels in the video imager and suggests that CMOS can displace CCDs for imagers having over a million pixels.

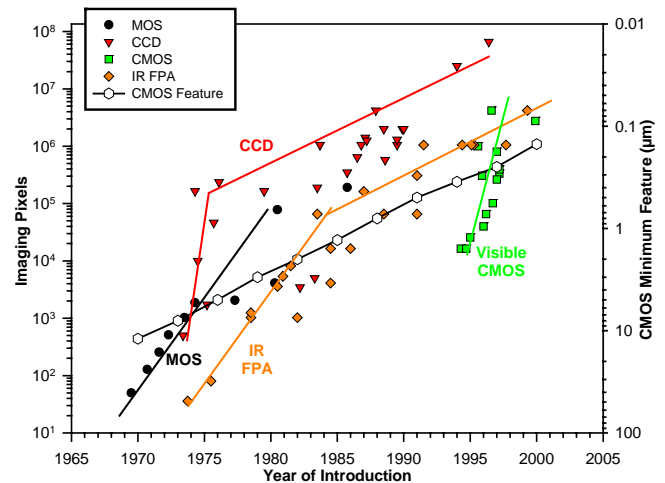


Figure 1. Chronology of imager pixels for MOS, CCD and CMOS imager technologies vs. CMOS minimum feature.

II. MULTIPLEXER READ NOISE: CCD VS. CMOS

A. Charge Coupled Device

Charge coupled device technology is mature with respect to production yield and performance. Both benchmarks are either at theoretical limits or practical levels significantly unchanged for several years. Figure 2 shows the schematic circuit for a typical CCD imager. The photo-generated carriers are first integrated in the well formed by a biased photogate and successively transferred via slow (vertical) and fast (horizontal) buried-channel CCD shift registers to the output node where the charge is subsequently converted to a voltage.

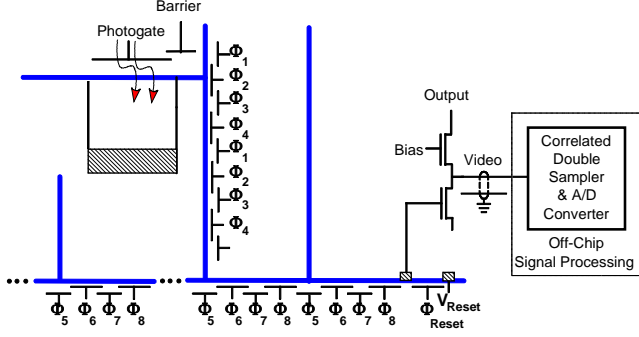


Figure 2. Architecture of representative CCD imager.

The sense node is usually formed by a floating diffusion with a small capacitance, C_{sense} , which modulates an output buffer (typically a source follower). Both the photovoltage and the floating diffusion's reset voltage are serially read, sampled and immediately subtracted from each other to eliminate the sense node's reset (kTC) noise via off-chip correlated double sampling (CDS). The readout conversion factor, S_v , in volts/electron is:

$$S_v = e(C_{sense} A_{sf})^{-1} \quad (1)$$

where A_{sf} is the voltage gain of the output buffer and e is the electron charge. C_{sense} is typically ~ 8 fF for astronomy CCDs and 10 to 12 fF for video CCDs because the output drive requirements are more difficult.

The dominant CCD noise sources include the white noise associated with optical and electrical signal input, shot noise from dark current, charge transfer noise, reset noise of the output structure, and thermal noise in the output amplifier [6,7]. After correlated double sampling [8] in the off-chip electronics, the minimum residual reset noise is:

$$N_{Post-CDS}(e^-) = \frac{2^{1/2}}{S_v} \sqrt{\int_0^{f_{max}} V_n^2(f) \left[\frac{1 - \cos 2\pi f t_{c-s}}{1 + (\pi f t_{c-s})^2} \right] df} \quad (2)$$

where t_{c-s} is the clamp-to-sample time, f_{max} is the output buffer bandwidth and $V_n^2(f)$ is the square of the spectral noise voltage of the amplifier MOSFET. The doubling of the output bandwidth, f_{max} , needed to support sequential readout of each pixel's signal and reset levels is represented by the prefactor $2^{1/2}$.

To predict the CCD noise as a function of array size, we first assume that ten time constants are needed to settle and accurately sample the video stream consisting of the signal and reset levels. This criterion assures 10 bit accuracy to not adversely perturb each pixel's reset level and thereby maximize efficacy of reset noise suppression. The minimum CCD video rate assuming one output channel is:

$$f_{video} = x \times y \times f_{frame} \times 2 \quad (3)$$

where x is the number of imager rows, y is the number of columns and f_{frame} is 30 Hz. We also optimize the load impedance for the output driver to maintain output buffer gain of 0.95. Finally using 12 fF sense capacitance, 50 pF capacitive load, and two phase CCD operation, we generate the noise analysis in Figure 3. The CCD transfer noise [9] is negligible because modern CCDs use buried channels. Without off-chip correlated double sampling, the predicted read noise is about 40 e^- , nearly independent of array size. By applying CDS, the read noise lowers via kTC noise reduction but becomes dependent on array size and video frequency. For an array comprising 0.3 million pixels, for example, the total read noise reduces to about 15 e^- at the video rate of about 35 MHz. The largest noise source is the output amplifier's thermal noise.

While the sense node capacitance can be lowered to somewhat reduce the input-referred read noise, practical considerations relating to maintenance of dynamic range and output buffer design often mandate instead reducing the frame rate. Astronomy CCDs, for example, are operated at < 100 kHz clock rate to limit the bandwidth. The concomitant band-limiting minimizes the output amplifier's thermal noise; the result is repeatable achievement of ~ 1 e^- read noise at a video rate of ~ 20 kHz. However, a one megapixel CCD thus operates at a frame rate of ~ 0.1 Hz. Since long exposures are often needed for astronomy, such low frame rates are not problematic. Other applications involving human gratification are not so forgiving.

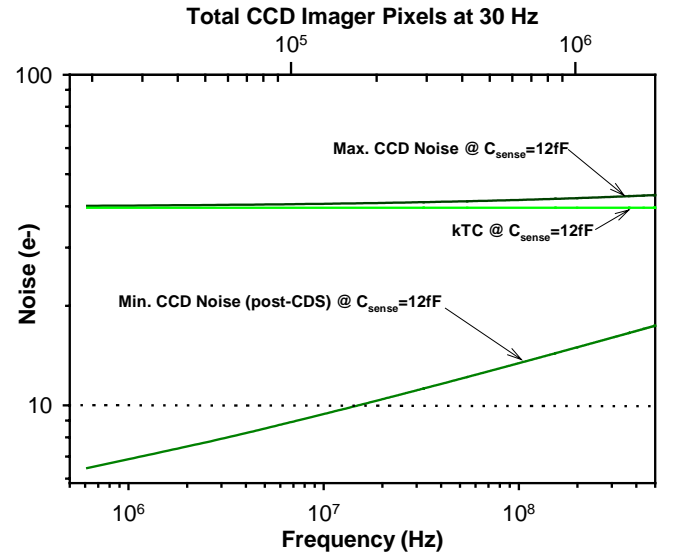


Figure 3. CCD noise at 30 Hz frame rate vs. video rate and imager pixels.

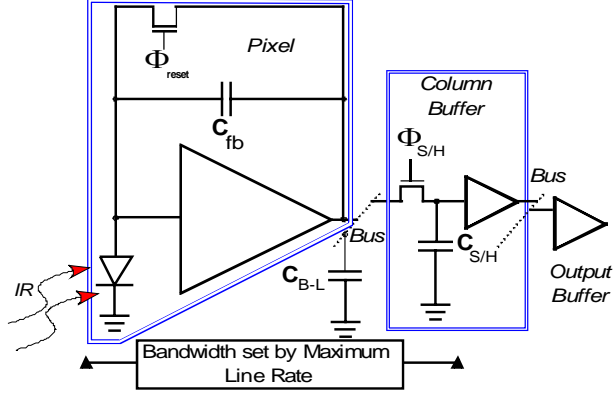


Figure 4. CMOS pixel-based amplifier with high sensitivity and noise bandlimiting.

B. CMOS-Based Imager

CMOS-based imagers for infrared and visible applications use either active [10] or passive [11] pixels. Active-pixel sensors (APS) exploit pixel-based amplification. On the other hand, the photogenerated signal from a passive pixel sensor (PPS) is instead read directly through a charge amplifier located in the column buffer that supports each column of the imaging array. Since passive pixel sensors consist of as few as two components (a photodiode and a MOSFET switch), circuit overhead is low and the optical collection efficiency (fill factor) is high even for monolithic devices. The large optical fill factor maximizes signal and minimizes cost by obviating the need for microlenses. Microlenses are a standard feature of CCD imagers.

Figure 4 shows a representative CMOS active pixel for infrared image sensors wherein the pixel amplifier supports a line-rate bandwidth rather than the much larger bandwidth of the output video; here the bus capacitance and amplifier output impedance facilitate the requisite band-limiting of the charge integrating amplifier's white noise. This can lower the minimum temporal noise because the requisite noise bandwidth is orders of magnitude larger than for a CCD. While the minimum read noise of a large format CCD is limited by the output amplifier's thermal noise as previously discussed, the CMOS paradigm supports lower temporal noise as long as the reset noise associated with the detector capacitance is appropriately mitigated. In effect, the low noise achieved with astronomy CCDs is upconverted to video bandwidths in a CMOS imager by the switched-capacitor nature of the multiplexer architecture.

By minimizing the amplifier $1/f$ noise via proper MOSFET sizing, the minimum read noise for the transimpedance amplifier shown in Figure 4 is [5]:

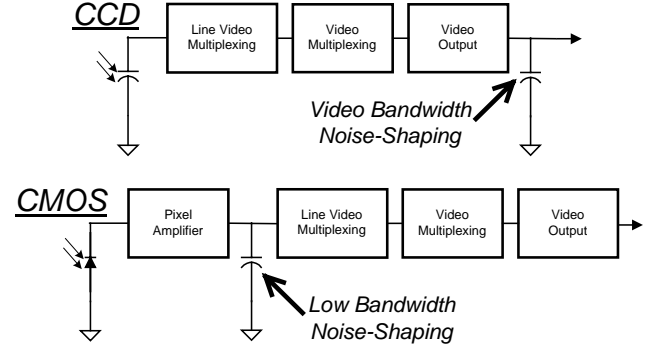


Figure 5. The CMOS paradigm with pixel-based amplification (e.g., CTIA) and noise bandlimiting.

$$N_{read} = \sqrt{\frac{nkTC_{fb}}{q^2} \frac{(C_{det} + C_{fb})^2}{C_L(C_{fb} + C_{det}) + C_{fb}C_{det}}} \quad (2)$$

where the prefactor n is one or two depending on single-ended or differential amplification, respectively, C_{fb} is the feedback capacitance including the Miller capacitance and integration capacitance, C_{det} is the detector capacitance, and C_L is the bandlimiting capacitance. The latter suppresses the wideband amp noise to match the line rate. Similar bandwidth optimization and noise reduction is available in the various other CMOS circuits used for detector interface. This capacitive transimpedance amplifier has yielded <30 e-read noise at 16 MHz data rate on an infrared 1024x1024 image sensor having $C_{det}=35$ fF detector capacitance, $C_{fb}=57$ fF feedback capacitance and $C_L=1.5$ pF [12].

A second CMOS advantage is that higher sensitivity can be achieved with relative ease. In the transimpedance amplifier of Figure 4, for example, a small feedback capacitance is readily implemented because the analog capacitor is manufactured in the overlying interconnect layers. Small capacitance translates to high photosensitivity, albeit with larger potential for pixel-to-pixel gain and offset variation. In the CCD, the sense capacitance and output buffer design are interrelated.

Figure 5 hence visually compares the key difference between CCD and CMOS readouts—the CMOS pixel amplifier supports a relatively low line rate rather than the full video rate as in a CCD. The requisite on-chip band-limiting thus represents much lower noise bandwidth than the CCD output amplifier must handle. Because the pixel-based amplification also minimizes vulnerability to EMI within the imager, the CMOS output buffer's wideband noise is rendered negligible, essentially independent of the actual video rate.

III. MEASURED IMAGER PERFORMANCE

The read noise of visible CMOS imagers having 1280x1024 (SXGA) and 1024x768 (XGA) formats was measured using test apparatus comprising either 14-b or 12-b A/D converter, a Preamble Model 1855 preamplifier with programmable bandwidth as large as 100 MHz and a personal computer with frame grabber. The SXGA's output driver rise and fall times of 3.5 ns and 7 ns, respectively, allowed operation to ~40 MHz. APS bandwidth, however, was set at a maximum of 100 kHz. Plotted in Figure 6 are read noise vs. frequency data from both the SXGA and the XGA along with CCD catalog data. The XGA's typical read noise of <30 e⁻ is comparable to the commercial CCD imagers except at higher frequencies where the XGA excels as expected by the simple theory. The SXGA, on the other hand, clearly excels due to its higher sensitivity of ~30μV/e⁻. In the basic operating mode used for digital still image capture, the read noise is <20 e⁻ to 25 MHz. While the visible astronomical imager data also shown in the figure represent the lowest read noise, the output rates for these data are incompatible with video applications.

Also plotted in the figure are the theoretical limits for CCD noise at C_{sense} of 8 fF and 12 fF, respectively. The CCD data points are roughly a factor of 2 higher from this practical limit, which assumes that 10 time constants of settling are needed at each video frequency. Since further improvements in CMOS imager read noise are likely as APS technology matures, the figure suggests that CMOS imagers should initially supplant CCDs for large formats.

We finally include measured read noise data from an infrared image sensor developed for astronomy [13]. In this case the read noise for the source follower APS circuit with C_{det}=35fF and conventional off-chip CDS is below 10 e⁻ for video rates below 2 MHz and as low as 8.5 e⁻ at 500 kHz.

IV. SUMMARY AND CONCLUSION

The availability of submicron mixed-signal CMOS is enabling development of monolithic visible imagers in CMOS because the available advanced photolithography now allows low-noise signal extraction and high performance photodetection at pixel pitch as small as 3.7μm [4]. This "sudden" emergence of CMOS imagers for sensing visible light is, hence, only one more consequence of Moore's Law, which predicts the ability to double transistor integration on each integrated circuit about every 18 months. Continuing advances in the resurgent MOS-based imaging technology may help CMOS supplant the incumbent CCD for many applications.

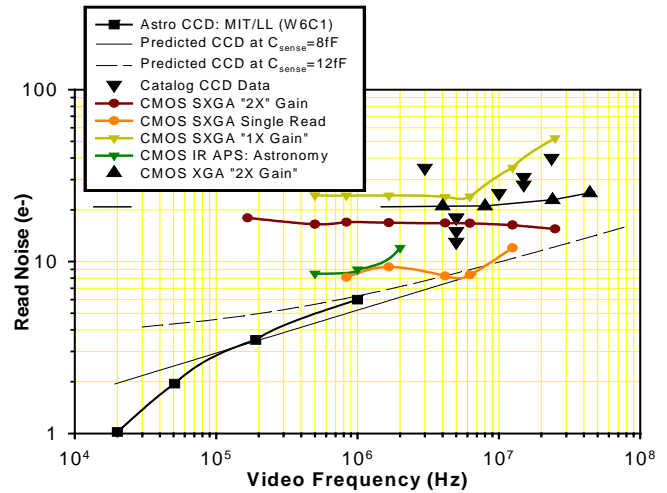


Figure 6. Measured CMOS imager and catalog CCD noise vs. frequency.

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